



H Happ Controls

106 Garlich Drive

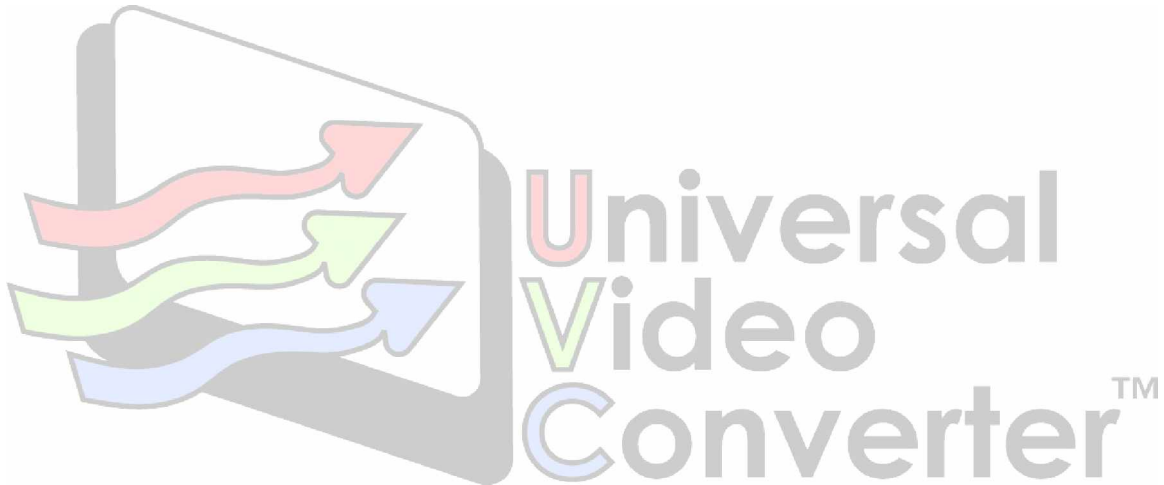
Elk Grove, IL 60007

Tel: 888-289-4277 / 847-593-6130

Fax: 847-593-6137

www.happcontrols.com

User Guide - Revision 2.01 01/23/04



.....



Table of Contents

Table of Contents.....	2
!!! IMPORTANT NOTE !!!	3
Overview	3
Legal Statements	3
Trouble Shooting	4
Input Resolutions.....	4
Output Resolutions.....	5
Cooling.....	6
Power	6
DIP Switch Settings	7
Configuration.....	8
LED Outputs.....	9
Logic Diagram	10
Revision History.....	11



!!! IMPORTANT NOTE !!!

This documentation applies to the 2.0 release of the uVC and the 02 revision of the PCB. The pinouts for the video output have changed with the H Sync and Video Ground being swapped to match pinouts on most monitors. Note, if you have 1.x release of the board with the 00 revision of the PCB, please note that you must swap the H Sync and Video Ground Pins on your monitor cable.

Overview

This is a very simple board that has only one function, to allow the display of PC based games on older arcade style monitors. The board needs to be an external device that requires no modification to the software running on the PC. It will handle one of three input resolutions (1024x768, 800x600 or 640x480) with a vertical refresh rate of 60Hz and output to one of two user selectable output modes (640x240@15.72KHz) or (640x384@24.9KHz). The coin-op monitors are RGB non-interlaced and run at 60Hz. The Input of the board will be a DBH-15 VGA analog VGA connector and the output is a 0.156" molex connector with pins for R, G, B, Ground and Syncs.

Legal Statements

The uVC board is copyright © 2003 by UltraCade Technologies, All Rights Reserved. The uVC board and it's algorithms are Patent Pending. uVC is a trademark of UltraCade Technologies. uVC is exclusively distributed by Happ Controls.



Trouble Shooting

The uVC should almost always work right out of the box. If you are having trouble getting an image to appear follow these steps:

- Verify that you have the proper output mode (try switching switch #3)
- Verify that you have the proper video cable attached to the monitor (note, if you have a 1.x board, make sure that they H and GND pins are correct, as they changed on 2.x boards)
- Try changing your sync from positive to negative, some monitors can't support positive sync.
- Try changing from composite to separate sync, some monitors can not support composite sync.

Input Resolutions

The uVC board supports multiple input resolutions

- Multiple PC VGA Input Formats
 - Input Resolutions
 - § 640x480
 - § 800x600
 - § 1024x768
 - Input Frequency
 - § Vertical 60Hz

Output Resolutions

The uVC board supports multiple output resolutions

- **Mode 1 - Low Resolution - CGA - (std resolution)**

○	Horizontal	Pixel Clock		73.626 ns
○	Horizontal	Active Pixels	640 pixels	47.121 μs
○	Horizontal	Total Pixels	864 pixels	63.613 μs
○	Horizontal	Front Porch	64 pixels	4.712 μs
○	Horizontal	Sync Width	60 pixels	4.418 μs
○	Horizontal	Back Porch	100 pixels	7.363 μs
○	Horizontal	Scan Rate	15.72 KHz	63.613 μs
○	Vertical	Line Clock		63.613 μs
○	Vertical	Active Lines	240 lines	15.267 ms
○	Vertical	Total Lines	262 lines	16.667 ms
○	Vertical	Front Porch*	3 lines	0.318 ms
○	Vertical	Sync Width	3 lines	0.191 ms
○	Vertical	Back Porch	14 lines	0.891 ms
○	Vertical	Refresh Rate	60 Hz	16.667 ms

- **Mode 2 - Med Resolution - EGA**

○	Horizontal	Pixel Clock		50.080 ns
○	Horizontal	Active Pixels	640 pixels	32.051 μs
○	Horizontal	Total Pixels	800 pixels	40.064 μs
○	Horizontal	Front Porch	16 pixels	0.801 μs
○	Horizontal	Sync Width	80 pixels	4.006 μs
○	Horizontal	Back Porch	64 pixels	3.205 μs
○	Horizontal	Scan Rate	24.96 KHz	40.064 μs
○	Vertical	Line Clock		40.064 μs
○	Vertical	Active Lines	384 lines	15.385 ms
○	Vertical	Total Lines	416 lines	16.667 ms
○	Vertical	Front Porch*	5 lines	0.200 ms
○	Vertical	Sync Width	5 lines	0.200 ms
○	Vertical	Back Porch	22 lines	0.881 ms
○	Vertical	Refresh Rate	60 Hz	16.667 ms

*Vertical Front Porch Timing is variable based on input frequency

•
•
•
•
•
•
•



Cooling

The board and chips use passive cooling. No heat sinks or fans are required. The board can perform in an environment up to 60 degrees Celsius.

Power

The board has a standard PC Hard Drive power connector, which brings in +12vdc, +5vdc, and Ground. The board contains an onboard power supply which will take the +12vdc and convert it to 3.3v and 1.8v needed in the logic. The +5vdc is passed onto the onboard 5v components.



DIP Switch Settings

8 – Sync Output Signal On=Composite *Off=HV Sync Separate

7 – Vertical Sync Polarity

Separate Sync -- *On=Positive Off=Negative

Composite Sync -- *On=Always Low Off=Always Hi

6 – Horizontal/Composite Sync Polarity *On=Positive Off=Negative

5:4 – Input Resolution

- *On/On = Auto Detect
- On/Off=VGA (640x480)
- Off/On=SVGA (800x600)
- Off/Off=XGA (1024x768)

3 – Output Display *On = Low Res (CGA) 15.75KHz Off = Med Res (EGA) 24.5KHz

2 – Output Delay Scan Lines

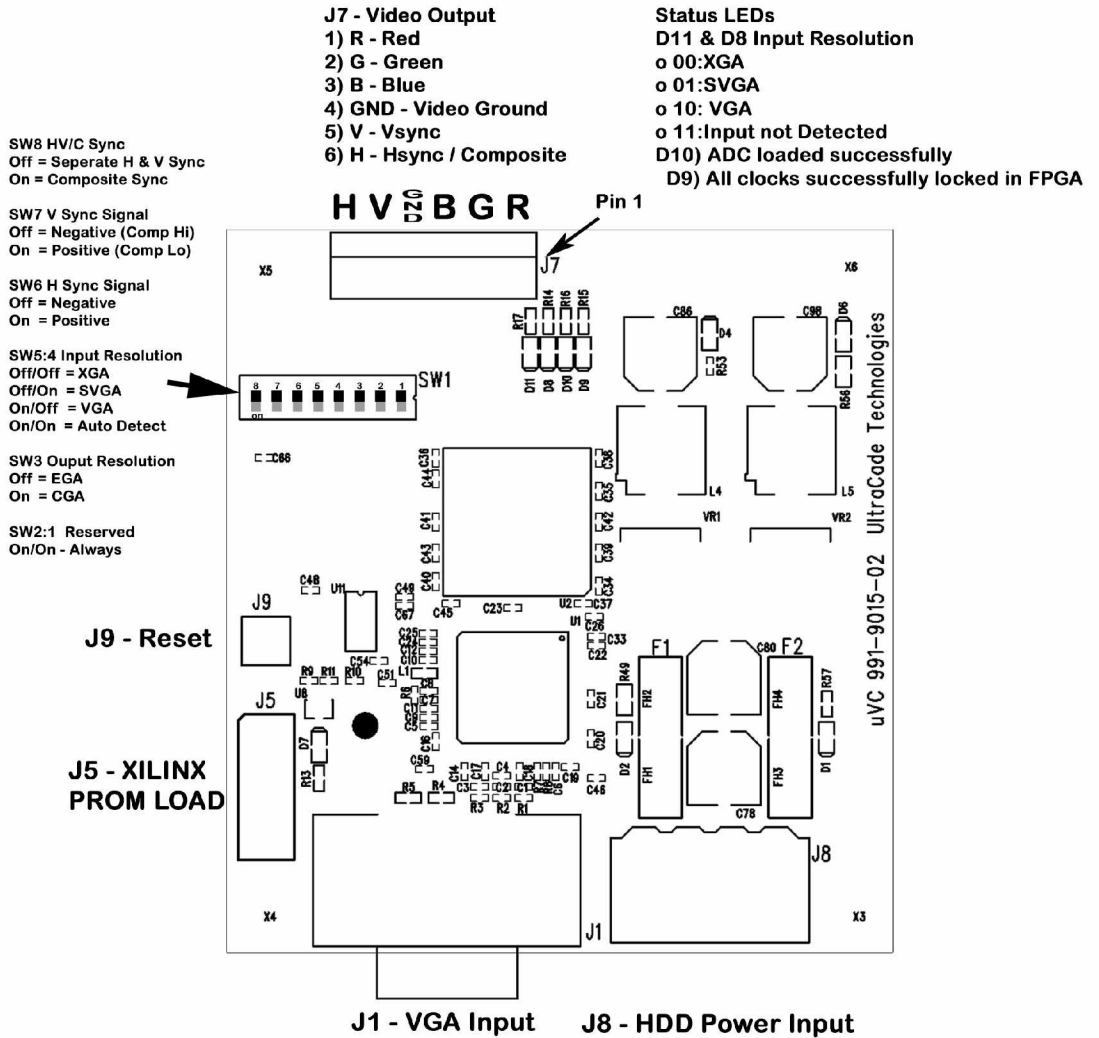
- *On = 8
- Off = 16

This should be set to as low as possible. If tearing appears on the bottom of the screen, increase the delay lines. If the top of the screen is wrapped around to the bottom, decrease the delay lines.

1 – Reserved

*denotes default settings

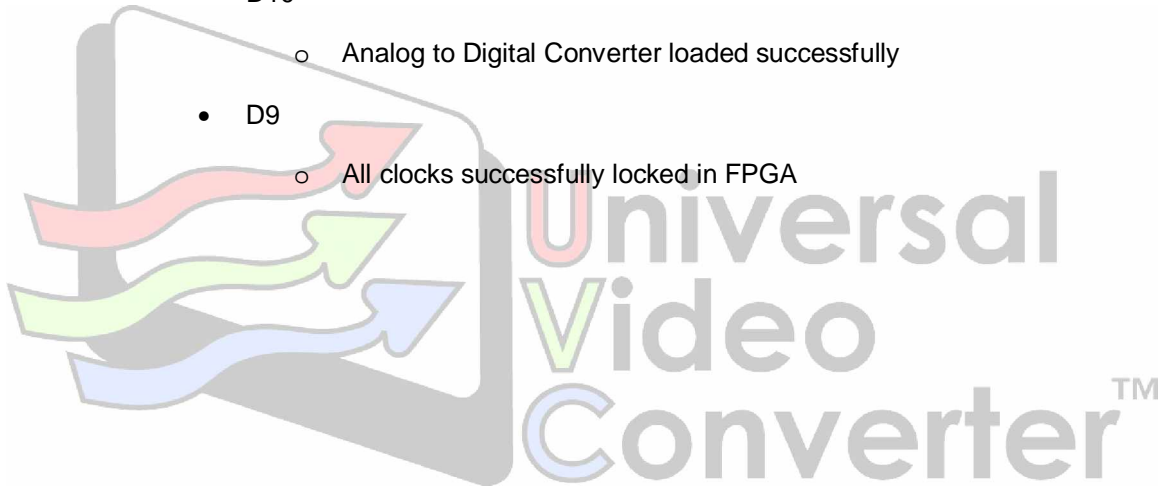
Configuration



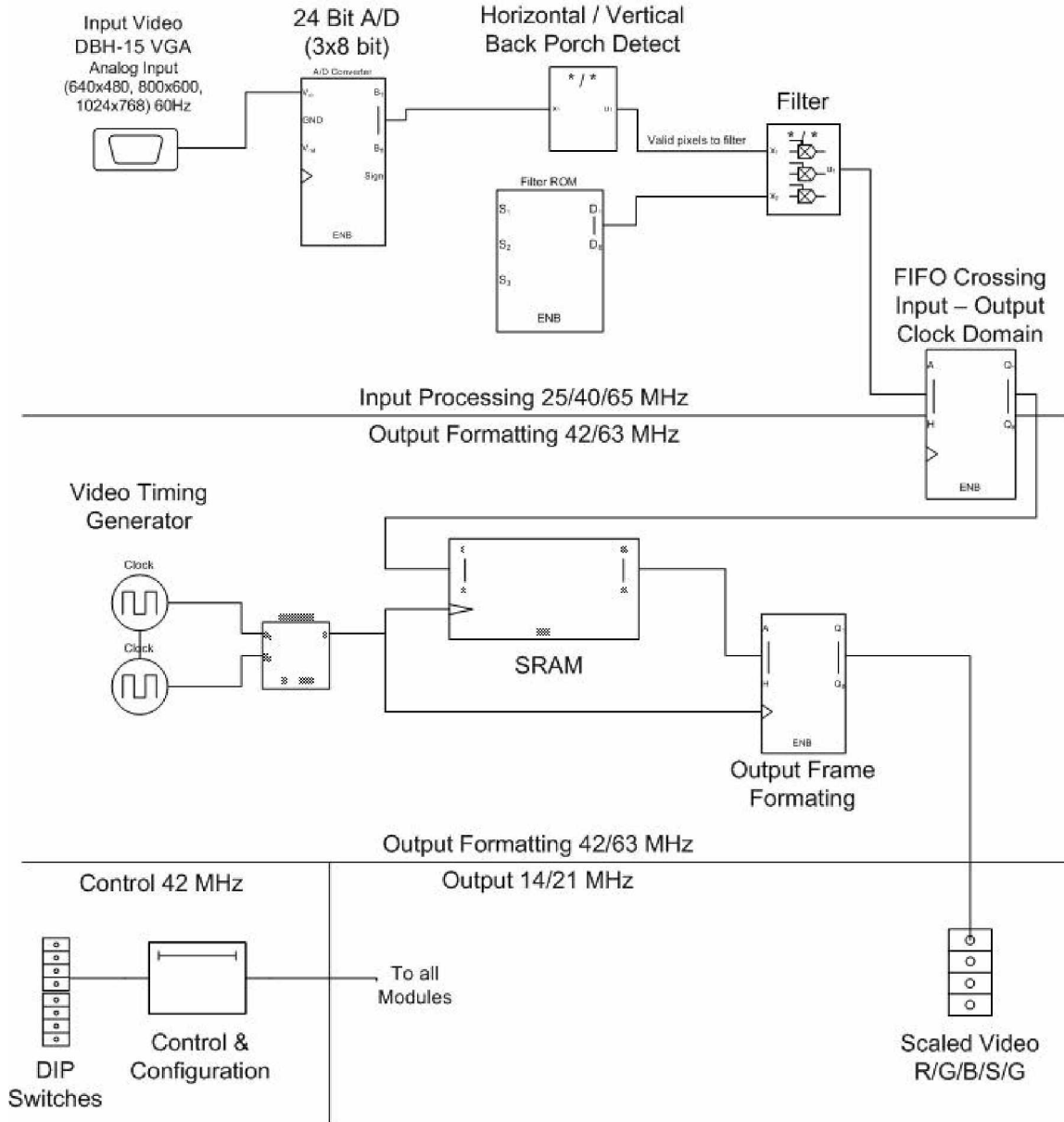
LED Outputs

There are four (4) LED's used for status display on board:

- D11 / D8
 - Input resolution (closest to dip switch)
 - § 00:XGA
 - § 01:SVGA
 - § 10: VGA
 - § 11:Input not Detected
- D10
 - Analog to Digital Converter loaded successfully
- D9
 - All clocks successfully locked in FPGA



Logic Diagram



Revision History

- January 23, 2004, DRF, Fixed J7 in wiring diagram
- December 14, 2003, DRF, Added Troubleshooting Section
- November 26, 2003, DRF, Update to version 2.00
 - PCB Revision 02
 - § Removal of unused LEDs
 - § Removal of unused pads for non-populated components
 - § Reset changed to external header instead of a push button
 - Output Pins reversed to match monitor input pinouts
 - BIOS screen now shows input and output resolution while syncing
- November 6, 2003, DRF, Update to version 1.81 ROM
 - Updated logic diagram
 - Updated switch settings
 - Added logo screen when switching modes or no input detected
- October 16, 2003, DRF, Updates to version 1.3 ROM
 - Automatic input resolution detection
 - Fix tear on SVGA -> CGA
- October 14, 2003, DRF, Updates to version 1.1 ROM
 - Update to remove use of jumpers
 - All settings via DIP switch
 - Additional of Polarity for H & V Syncs



- October 13, 2003, DRF, Updates to version 0.20 ROM
 - Input Horizontal Timing
 - Addition of new switch functions on chart
 - Correction to input resolution Switch notes
 - Output Timing update
 - Power Update
- October 10, 2003, DRF, Initial Revision to version 0.18 ROM

